In the Claims:

Claims 1-3 (Canceled).

4. (Currently amended) A method of forming a vertical metal-oxide-semiconductor field effect transistor **[[**MOSFET**]]**, comprising the steps of:

implanting base region dopants of second conductivity type into an active portion of a semiconductor substrate having a drift region of first conductivity type therein;

forming a first mask having openings therein on the active portion of the semiconductor substrate;

implanting shielding region dopants of second conductivity type into the active portion of the substrate, using the first mask as an implant mask;

driving-in the implanted base and shielding region dopants to define a base region and a plurality of base shielding regions that extend laterally underneath the first mask and vertically through the base region and into the drift region;

etching first and second deep trenches into the semiconductor substrate to define a drift region mesa therebetween, using the first mask as an etching mask;

forming first and second insulated source electrodes in the first and second trenches, respectively;

implanting source region dopants of first conductivity type into the drift region mesa;

driving-in the implanted source region dopants to define a source region in the base region;

forming a shallow trench that extends in the drift region mesa and has a sidewall extending adjacent the base and source regions;

forming an insulated gate electrode in the shallow trench; and

forming a source electrode that electrically connects the first and second insulated source electrodes, the source region and the base region together.

5. (Original) A method of forming a vertical power device, comprising the steps of:

forming first and second stripe-shaped trenches that extend in parallel and in a first direction across a semiconductor substrate having a drift region therein that extends adjacent a face thereof;

forming first and second insulated electrodes in the first and second stripe-shaped trenches, respectively;

forming first and second base regions of second conductivity type that each extend from a sidewall of said first stripe-shaped trench to an opposing sidewall of said second stripe-shaped trench and define a respective P-N junction with the drift region;

forming first and second source regions of first conductivity type in said first and second base regions, respectively;

forming a source electrode that extends on the first face and is electrically connected to said first and second insulated electrodes and to said first and second source regions; and

forming an insulated gate electrode that extends in a second direction across the first face of said semiconductor substrate that is orthogonal to the first direction.

6. (Original) The method of Claim 5, wherein said step of forming an insulated gate electrode comprises forming an insulated gate electrode that extends opposite the first and second base regions and the drift region and is positioned so that during forward on-state conduction in the vertical power device, majority carriers provided by the first and second source regions flow across the first and second base regions in a direction parallel to the first and second stripe-shaped trenches.